REMARKS

This Amendment is filed in response to the Office Action mailed Sept. 8th, 2004. All objections and rejections are respectfully traversed.

Claims 1-37 are pending in the case.

Claims 1, 11, 19, 20, 21, 22, 27, 32, 33, 34 have been amended to better claim the invention.

Claim Rejections – 35 U.S.C. §102

At paragraphs 1-2 of the Office Action claims 1, 7, 11, and 19-21, and 35-37 were rejected under 35 U.S.C. §102(e) as being anticipated by Greim et al., U.S. Patent No. 6,163,829 (hereinafter Greim).

The present invention as set forth in representative claim 1 recites:

> A system configured to acknowledge and service an interrupt issued to a processor of an intermediate node, the system comprising:
>
> an external device coupled to a high latency path, the external device generating a pulsed interrupt signal for each type of interrupt supported by the processor;
>
> an interrupt multiplexing device accessible by the processor over a fast bus;
>
> ***a low latency path coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device***; and
>
> a status bit stored within the interrupt multiplexing device, the status bit adapted for assertion whenever the pulsed interrupt signal is detected at the interrupt multiplexing device,

wherein, ***in response to the pulsed interrupt signal, the interrupt multiplexing device issues a level sensitive interrupt (LSI) signal to the processor over the fast bus, the LSI signal remaining asserted until the interrupt is acknowledged by the processor by clearing the status bit.***

Greim discloses an interrupt handler that distributes interrupts among a plurality of processors. First, external devices issue interrupts on an external bus (VME bus, Fig 4, Item 12), to a VME interface (Fig 4, item 18), which intern conducts them to an interrupt controller (Fig 4, item 82). These interrupt signals are edge sensitive, that is, they trigger action on a rising edge and then remain asserted until acknowledged. Upon receiving an interrupt signal, the processor accesses stored information about the interrupt by reading registers over a local bus (Fig 6, item 22) and then services the pending interrupt (col. 29, lines 10-26). An acknowledgment manager (Fig 6, item 110) in the interrupt controller monitors the CPU and upon detecting an interrupt has been serviced, generates an acknowledgement signal and sends it to the external device over the system bus. (Col 25, lined 8-12). Upon receiving the acknowledge, the interrupt signals are de-asserted.

Applicant respectfully urges that Griem does not show Applicant's claimed invention relating to "***a low latency path coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device***" and ***"in response to the pulsed interrupt signal, the interrupt multiplexing device issues a level sensitive interrupt (LSI) signal to the processor over the fast bus, the LSI signal remaining asserted until the interrupt is acknowledged by the processor by clearing the status bit."***

The Applicant's claimed novel invention reduces delays in interrupt handling by moving acknowledge operations closer to the processor. To accomplish this the Applicant used **two types** of interrupt signals, pulsed signals that do not require acknowledgement, and LSI signals that remain asserted until acknowledged. By pulsing an interrupt from the external device to the interrupt multiplexing device, an acknowledge operation over a slow path can be avoided. Yet an acknowledgment operation is still necessary to interface with the processor and ensure proper operation of the interrupt. Therefore the "***in response to the pulsed interrupt signal, the interrupt multiplexing device issues a level sensitive interrupt (LSI) signal to the processor over the fast bus, the LSI signal remaining asserted until the interrupt is acknowledged by the processor by clearing the status bit.***" This local acknowledge can be done much quicker than an acknowledge all the way out to the external device.

Griem only discloses a **single** type of interrupt signal, an edge-sensitive interrupt signal that remains asserted until acknowledged. Thus Griem is completely silent on converting a pulsed interrupt signal into an LSI signal. Further, Griem does not acknowledge an interrupt **at** its interrupt controller, but rather issues an acknowledge signal **from** its interrupt control to the external device via the system bus. This is the type of high latency operation that the Applicant has sought to avoid.

Accordingly, the Applicant respectfully urges that Griem is legally insufficient to anticipate the presently claims under 35 U.S.C. §102 because of the absence of Appli-

cants' claimed novel "***a low latency path coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device***" and ***"in response to the pulsed interrupt signal, the interrupt multiplexing device issues a level sensitive interrupt (LSI) signal to the processor over the fast bus, the LSI signal remaining asserted until the interrupt is acknowledged by the processor by clearing the status bit."***

Claim Rejections – 35 U.S.C. §103

At paragraphs 3-5 of the Office Action claims 2-6 and 12-17 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Greim and Shek et al., U.S. Patent No. 6,185,652 (hereinafter Shek).

Applicant respectfully notes that claims 2-6 and 12-17 are dependent from independent claims that are believed to be in condition for allowance. Accordingly, the dependant claims are believed to be in condition for allowance.

At paragraph 6 of the Office Action claim 18 was rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Greim, Shek, and Ecclesine, U.S. Patent No. 5,983,275 (hereinafter Ecclesine).

Applicant respectfully notes that claim 18 is dependent from an independent claim that is believed to be in condition for allowance. Accordingly, the dependant claim is believed to be in condition for allowance.

At paragraph 7 of the Office Action claims 8 and 9 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Greim and Wu et al., U.S. Patent No. 5,682,483 (hereinafter Wu) or Griem and the admitted art.

Applicant respectfully notes that claims 8 and 9 are dependent from an independent claim that is believed to be in condition for allowance. Accordingly, the dependant claims are believed to be in condition for allowance.

At paragraph 8 of the Office Action claims 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Greim and Shatas et. al, U.S. Patent No. 5,983,275 (hereinafter Shatas).

Applicant respectfully notes that claim 10 is dependent from an independent claim that is believed to be in condition for allowance. Accordingly, the dependant claim is believed to be in condition for allowance.

At paragraph 9 of the Office Action claims 1,7, and 19-21 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Greim and Swanstrom, U.S. Patent No. 5,754,884 (hereinafter Swanstrom).

Swanstrom describes a direct memory access (DMA) controller which services interrupt requests so that while a CPU is servicing one interrupt request the CPU cannot be interrupted by another interrupt request (Col. 10, lines 25-42). The interrupt requests and corresponding acknowledge (clear) actions are transferred from the processor, over a PCI bus, to the DMA controller (Col. 11, lines 28-37, 52-53).

Applicant respectfully urges that the combination of Swanstrom and Griem does not show Applicant's claimed invention relating to "***a low latency path coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device***" and ***"in response to the pulsed interrupt signal, the interrupt multiplexing device issues a level sensitive interrupt (LSI) signal to the processor over the fast bus, the LSI signal remaining asserted until the interrupt is acknowledged by the processor by clearing the status bit***."

Both Griem and Swanstrom are silent concerning converting pulsed interrupt signals to LSI signals. Further, both Griem and Swanstrom are silent concerning acknowledging an interrupt **at** the interrupt controller, but eather send acknowledge signal **from** its interrupt control to the external device via the system bus.

Accordingly, Applicant respectfully urges that Swanstrom and Greim, taken either signally or in combination, are legally precluded from anticipating Applicant's claimed novel invention under 35 U.S.C. 103(a) because of the absence of Applicant's "***a low latency path coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device***" and ***"in response to the pulsed interrupt signal, the interrupt multiplexing device issues a level sensitive interrupt (LSI) signal to the processor over the fast bus, the LSI signal remaining asserted until the interrupt is acknowledged by the processor by clearing the status bit***."

At paragraph 10 of the Office Action claims 2-6, and 12-17 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Swanstrom, Greim and Shek.

Applicant respectfully notes that claims 2-6, and 12-17 are dependent from independent claims that are believed to be in condition for allowance. Accordingly, the dependant claims are believed to be in condition for allowance.

At paragraph 11 of the Office Action claims 8 and 9 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Swanstrom, Greim and Wu or Swanstrom, Griem and admitted prior art.

Applicant respectfully notes that claims 8 and 9 are dependent from an independent claim that is believed to be in condition for allowance. Accordingly, the dependant claims are believed to be in condition for allowance.

At paragraph 12 of the Office Action claim 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Swanstrom, Greim and Shata.

Applicant respectfully notes that claim 10 is dependent from an independent claim that is believed to be in condition for allowance. Accordingly, the dependant claim is believed to be in condition for allowance.

At paragraph 13 of the Office Action claim 18 was rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Swanstrom, Greim, Shek, and Eclesine.

Applicant respectfully notes that claim 18 is dependent from an independent claim that is believed to be in condition for allowance. Accordingly, the dependant claim is believed to be in condition for allowance.

At paragraph 14 of the Office Action claims 22-24, 27-29, and 32-34 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Swanstrom, Greim and Okbay et al., U.S. Patent No. 6,606,677 (hereinafter Okbay).

The present invention as set forth in representative claim 22 recites:

> A method for acknowledging and servicing an interrupt issued to a processor, the method comprising:
>
> generating a pulsed interrupt signal at an external device;
>
> ***transporting the pulsed interrupt signal to an interrupt multiplexing device over a first low latency path that couples the external device to the interrupt multiplexing device***;
>
> asserting a status bit in the interrupt multiplexing device corresponding to the interrupt in response to detecting the pulsed interrupt signal;
>
> ***issuing to the processor over a second low latency path, in response to the pulsed interrupt signal, a level sensitive interrupt (LSI) signal, the LSI signal remaining asserted until the interrup tis acknowledged by the processor***;
>
> reading the status bit over the second low latency path by an interrupt handler internal to the processor; and
>
> ***clearing the status bit in response to the reading of the status bit to effectively acknowledge the interrupt.***

Okbay discloses an interruptible bridge which interconnects two PCI busses. All interrupt requests and acknowledgements apparently pass between the two PCI busses and the interruptible bridge.

Applicant respectfully urges that Griem does not show Applicant's claimed invention relating "***transporting the pulsed interrupt signal to an interrupt multiplexing device over a first low latency path that couples the external device to the interrupt multiplexing device***" and "***issuing to the processor over a second low latency path, in response to the pulsed interrupt signal, a level sensitive interrupt (LSI) signal, the LSI signal remaining asserted until the interrupt is acknowledged by the processor***" and "***clearing the status bit in response to the reading of the status bit to effectively acknowledge the interrupt.***"

Okbay teaches a conventional system where interrupt requests and acknowledgements travel along PCI busses.

All the references, including Okbay are silent concerning converting pulsed interrupt signals to LSI signals. Further, all the references, including Okbay are silent concerning acknowledging an interrupt **at** an interrupt controller.

Accordingly, Applicant respectfully urges that Swanstrom and Greim and Okbay, taken either signally or in combination, are legally precluded from anticipating Applicant's claimed novel invention under 35 U.S.C. 103(a) because of the absence "***transporting the pulsed interrupt signal to an interrupt multiplexing device over a first low latency path that couples the external device to the interrupt multiplexing device***" and

"issuing to the processor over a second low latency path, in response to the pulsed interrupt signal, a level sensitive interrupt (LSI) signal, the LSI signal remaining asserted until the interrupt is acknowledged by the processor" and ***"clearing the status bit in response to the reading of the status bit to effectively acknowledge the interrupt."***

At paragraph 15 of the Office Action claims 25 and 30 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Swanstrom, Greim and Okbay, and Shek.

Applicant respectfully notes that claims 25 and 30 are dependent from a independent claims that are believed to be in condition for allowance. Accordingly, the dependant claims are believed to be in condition for allowance.

At paragraph 16 of the Office Action claims 26 and 31 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Swanstrom, Greim and Okbay, and Ecclesine.

Applicant respectfully notes that claims 26 and 31 are dependent from a independent claims that are believed to be in condition for allowance. Accordingly, the dependant claims are believed to be in condition for allowance.

All independent claims are now believed to be in condition for allowance.

All dependant claims are believed to be dependant from allowable independent claims.

The Applicant therefore respectfully requests favorable action.

The Applicant earnestly solicits the Examiner to contact the undersigned by telephone at 617-951-3078 to advance the prosecution of the application in any respect.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,

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